Atty Docket No. JCLA5775 **Serial No. 09/974,559**

REMARKS

Present Status of the Application

The Office Action rejected claims 1-14, wherein claims 4-7 and 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if written in independent form including all of the limitations of these claim and any intervening claims. Specifically, the Office Action rejected claims 1-3 and 8-10 under 35 U. S. C. 103(a) as being unpatentable over U. S. Patent 6,269,443 B1 (Poisner et al., hereinafter referred to Poisner) in view of AMD Duron Processor Data Sheet (hereinafter, referred to AMD). Claims 1-14 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion for Independent Claim Rejections under 35 USC 103 (a)

1. *Independent Claims 1 and 8 are rejected under 35 U. S. C. 103(a) as being unpatentable over Poisner in view of AMD.*

Regarding to Independent Claim 1, Poisner discloses a system capable of automatically reading-out a multiple value of clock frequency and adjusting a processor clock speed multiplier accordingly, but doesn't explicitly disclose utilizing a serial initialization packet (SIP) protocol for communication between the processor and the chipset. AMD discloses that SIP is a well known that is used to communicate configuration information from a chipset to a processor (pages 34 and 35). It would have been obvious to one of ordinary skill in the art to use the well known SIP protocol for communication between the processor and the chipset in the Poinser

system to ensure compatibility with conventional computer components.

Regarding to Independent Claim 8, Poisner discloses a method of automatically reading-out a multiple value of clock frequency and adjusting a processor clock speed multiplier accordingly, but doesn't explicitly disclose utilizing a serial initialization packet (SIP) protocol for communication between the processor and the chipset. AMD discloses that SIP is a well known that is used to communicate configuration information from a chipset to a processor (pages 34 and 35). It would have been obvious to one of ordinary skill in the art to use the well known SIP protocol for communication between the processor and the chipset in the Poinser system to ensure compatibility with conventional computer components.

In response thereto, applicants respectfully transverse the objection based on the following arguments and thus withdrawal of objections to the independent claims 1 and 8 is respectfully requested. As recognized by the examiner, Poiners fails to utilize a serial initialization packet (SIP) protocol for communication between the processor and the chipset. Poisner utilizes an apparatus for automatically selecting central process unit (CPU) clock frequency multiplier. In addition, the apparatus comprises a processing failure detection circuit and a clock frequency multiplier indicator circuit. Instead, the present application can automatically reading-out the multiple value of clock frequency on system bus by implementing a chipset's attempting to synchronize with a CPU in a SIP protocol that uses a preset multiple value of clock frequency as a parameter, as disclosed in the "ABSTRACT OF THE DISCLOSURE" IN THE SPECIFICATION." As a result, the implemented means of the

present application is distinct from that of Poisner. Furthermore, the examiner alleged that the combination of Poisner and AMD would render the independent claims 1 and 8 obvious because the AMD discloses that SIP is a well known and used to communicate configuration information from a chipset to a processor (pages 34 and 35). However, throughout the brochure of AMD, especially in pages 34 and 35, there just only discloses "Processors and Northbridges are designed to adhere to the following protocol and do not require motherboard intervention." as disclosed in the last sentence in page 34. In other words, the AMD doesn't disclose any phrase pertaining to "a chipset's attempting to synchronize with a CPU in a SIP protocol that uses a preset multiple value of clock frequency as a parameter" as disclosed in the present application, nor does Poisner. Therefore, in view of Poisner and AMD, one of ordinary skill in the art would have no reason to make such a combination. Moreover, the combination couldn't be made physically because the apparatus of Poisner would not work with the AMD's SIP due to a non-used SIP in Poisner.

The citation fails to disclose "a chipset, wherein the chipset is capable of repeatedly selecting a multiple value of clock frequency to serve as a parameter in a serial initialization protocol until a synchronizing multiple clock frequency is found" as claimed and mainly featured in the independent claim 1. Likewise, the citation fails to disclose "using said preset multiple value of clock frequency as a parameter in serial initialization protocol" as claimed and mainly featured in the independent claim 8. According to the foregoing discussions and requirements established to a *prima facie* case of obviousness, the combination of Poisner and AMD would not render the independent claims 1 and 8 obvious. That is, the independent claims 1 and 8 are patentable over Poisner in view of AMD.

Discussion for Dependent Claim Rejections under 35 USC 103 (a)

2. Regarding to claims 2 and 3, Poisner discloses that the chipset tries to implement the fastest possible clock frequency multiplier at first and then tries successively smaller multipliers until the processor is able to operate normally (col. 4, lines 10-17) Poinser doesn't explicitly state that a counter is used to generate the successively smaller multipliers in the system. However, Poinsner inherently disclose a counter since some sort of counting means would have to be used in order to produce the successively smaller multipliers in the system.

Regarding to claims 9 and 10, Poisner discloses that the chipset tries to implement the fastest possible clock frequency multiplier at first and then tries successively smaller multipliers until the processor is able to operate normally (col. 4, lines 10-17) Poinser doesn't explicitly state that a counter is used to generate the successively smaller multipliers in the system. However, Poinsner inherently disclose a counter since some sort of counting means would have to be used in order to produce the successively smaller multipliers in the system.

In response thereto, applicants respectfully transverse the objection based on the following arguments and thus withdrawal of objections to the dependent claims 2-3 and 9-10 are respectfully requested. From col. 4, lines 10-17 in Poinser, there doesn't disclose any phrase pertaining to "the system further includes a counter is capable of generating a new counting value after each failed to attempting to synchronize" as claimed in claims 2 and 9. Although the examiner alleged that Poinsner inherently disclose a counter since some sort of

counting means would have to be used in order to produce the successively smaller multipliers in the system, the phrase of "Poinsner inherently disclose a counter" in the examiner's allegation is regarded as the examiner's hypothetical allegation because of failing to provide a convincing evidence. Moreover, Poinsner fails to disclose "multiple value of clock frequency is changed by according to said counting value" as claimed in claims 3 and 10. Accordingly, dependent claims 2-3 and 9-10 are patentable over Poinsner.

In addition, dependent claims 2-3 and 9-10, which directly or indirectly depend on their independent base claims 1 and 8, are patentable as a matter of law, for at least the reason that the dependent claims 2-3 and 9-10 contain all features of their base independent claim 1 and 8.

For at least the foregoing reasons, Applicant respectfully submits that claims 1-14 patently define over the prior art references, and should be allowed. Reconsideration of claims 1-14 and withdrawal of objections to claims 1-14 are respectfully requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-14 of the invention patently define over the prior art and are in proper condition for allowance. Reconsideration of claims 1-14 and the present application is respectfully requested. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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